

PIN NAME	40-pin DIP PIN No.	42-pin SDIP PIN No.	DESCRIPTION
PC6/PWM14/VTTL, PC7/PWM15/HTTL	32, 33	33, 34	These two port C I/O lines are shared with the PWM and Sync Signal Processor. Configuration for use are set by the Configuration register 1 (\$0A) and Configuration register 2 (\$0B).
PD0/SDA, PD1/SCL	24, 25	25, 26	These two port D I/O lines are shared with the M-Bus lines SDA and SCL. When configured as M-Bus lines in Configuration register 2 (\$0B), these pins become +5V open-drain pins.
PWM0 to PWM7	3-1, 38-34	3-1, 40-38, 36, 35	These eight pins are dedicated for the 8-bit PWM channel 0 to 7.
HSYNC, VSYNC	39, 40	41, 42	These two pins are for video sync signals input from the host computer. The polarity of the input signals can either be positive or negative. These two pins contain internal Schmitt triggers as part of their inputs to improve noise immunity

2.2 Pin Assignments

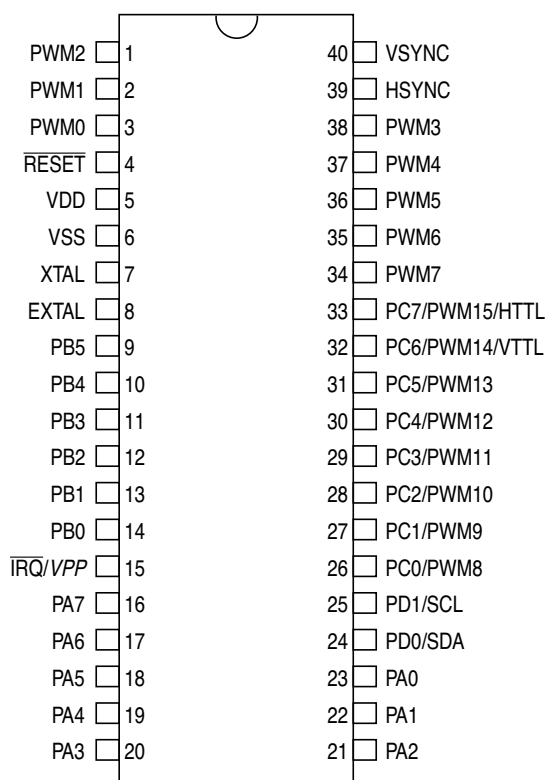


Figure 2-1 Pin Assignment for 40-pin DIP Package

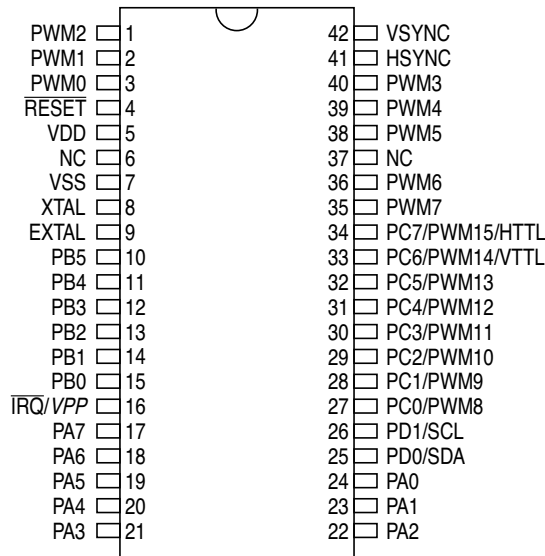


Figure 2-2 Pin Assignment for 42-pin SDIP Package

2.3 INPUT/OUTPUT PORTS

In the User Mode there are 24 bidirectional I/O lines arranged as 4 I/O ports (Port A, B, C, and D). The individual bits in these ports are programmable as either inputs or outputs under software control by the data direction registers (DDRs). Also, if enabled by software, Port C and D will have additional functions as PWM outputs, M-Bus I/O and Sync Signal Processor outputs.

2.3.1 Port A

Port A is an 8-bit bidirectional port which does not share any of its pins with other subsystems. The Port A data register is at \$00 and the data direction register (DDR) is at \$04. Reset does not affect the data register, yet clears the data direction register, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.

2.3.2 Port B

Port B is a 6-bit bidirectional port which does not share any of its pins with other subsystems. PB2 to PB5 are +10V open-drain port pins. The Port B data register is at \$01 and the data direction register (DDR) is at \$05. Reset does not affect the data register, yet clears the data direction register, thereby returning the ports to inputs. Writing a one to a DDR bit sets the corresponding port bit to output mode.