

PIN NAME	44-pin QFP PIN No.	DESCRIPTION
PB0-PB7	25-18	These eight I/O lines comprise port B. The state of any pin is software programmable. All port B lines are configured as input during power-on or external reset. PB7 is also used as the RSPWM counter reset input when PB7 is set as an input pin and the counter reset enable bit is set in the GPWM register (bit 6 of \$0010).
PC0-PC7	17-10	These eight I/O lines comprise port C. The state of any pin is software programmable. All port C lines are configured as input during power-on or external reset. PC0-PC5 become keyboard interrupt input pins when the corresponding bits are set in the Keyboard Interrupt register (\$001E). PC6 and PC7 are SDA and SCL respectively, when used for the software supported M-Bus Interface.
SDA, SCL	2, 3	These are the hardware M-Bus interface data and clock lines.
TCAP	9	This input pin controls the input capture function of the 16-bit free-running timer.
TCMP	8	This output pin indicates when a timer compare is successful.
GPWM	7	This is the output pin of the General purpose PWM.
RSA, RSB	5, 6	These are the two excursive outputs of the Raster Positioning PWM
RCLK	4	This is the input clock to drive the RSPWM counter.
HSYNC, VSYNC	40, 41	These two input pins are for the video sync signals from the host computer.
CSYNC	42	This is the Composite sync signal input from the host computer.
SAM	43	This is the output of an sample signal from the Sync Signal Processor.
HTTL, VTTL	44, 1	These are the output from the HSYNC and VSYNC inputs or the signals separated from CSYNC input.

## 2.2 Pin Assignment

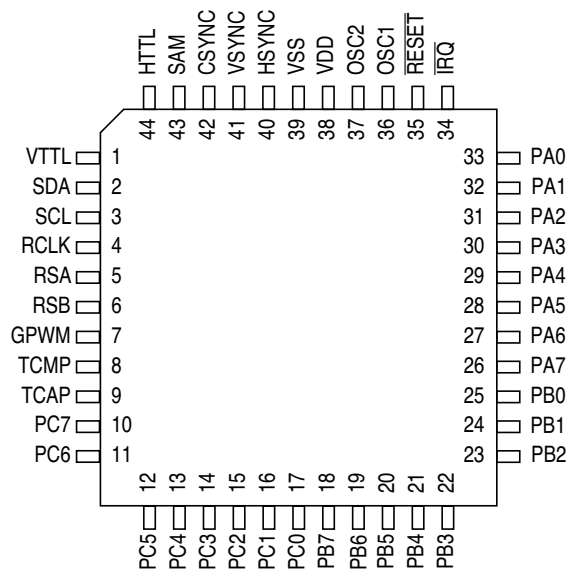


Figure 2-1 Pin Assignment for 44-pin QFP Package