1.6 Functional Pin Descriptions

Figure 1-3, **Figure 1-4**, **Figure 1-5**, and **Figure 1-6** show the pin assignments for the available packages. A functional description of the pins follows.

NOTE: *A line over a signal name indicates an active low signal. For example, RESET is active high and $\overline{RESET}$ is active low.*

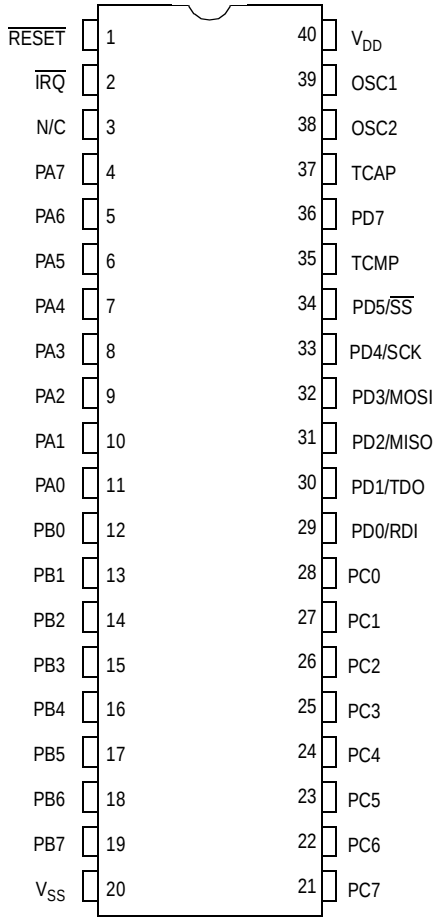

Figure 1-3. 40-Pin PDIP Pin Assignments

NOTE: *If MC68HC705C9A devices are to be used in the same socket, pin 3 should be tied to V_{DD}.*

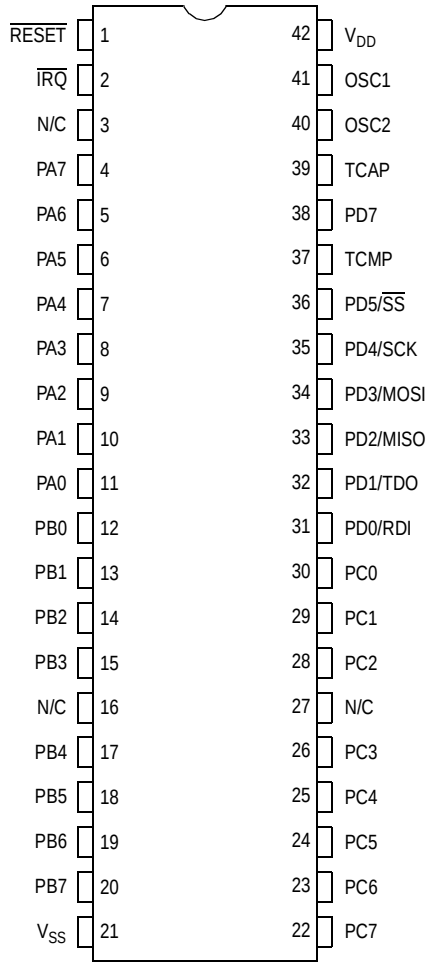

Figure 1-4. 42-Pin SDIP Pin Assignments

NOTE: *If MC68HC705C9A devices are to be used in the same socket, pin 3 should be tied to V_{DD}.*

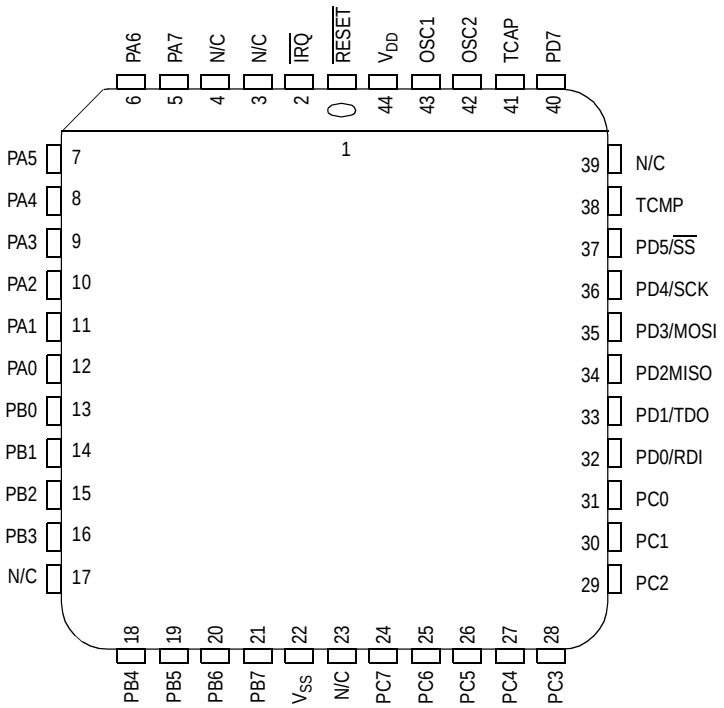

Figure 1-5. 44-Lead PLCC Pin Assignments

NOTE: *The 44-pin PLCC pin assignment diagram is for compatibility with the MC68HC705C9A. However, if MC68HC705C9A devices are to be used in the same socket, pin 3 should be tied to V_{DD}.*

For compatibility with MC68HC05C4A/C8A/C12A devices in 44-pin PLCC, tie pins 17 and 18 together, and tie pins 39 and 40 together.

For compatibility with MC68HC705C8A 44-pin PLCC device, three sets of pins should be tied together: pins 17 and 18, pins 39 and 40, and pins 3, 4, and 44.

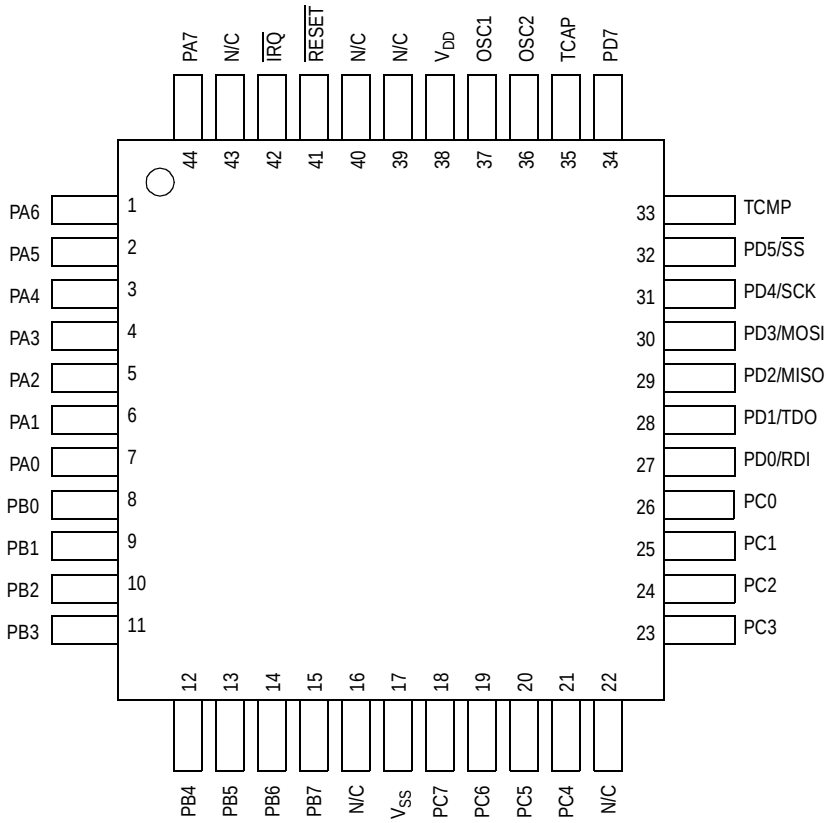

Figure 1-6. 44-Pin QFP Pin Assignments

NOTE: *If MC68HC705C9A devices are to be used in the same socket, pin 43 should be tied to V_{DD}.*

1.6.1 V_{DD} and V_{SS}

Power is supplied to the MCU using these two pins. V_{DD} is the positive supply and V_{SS} is ground.

1.6.2 $\overline{IRQ}$

This interrupt pin has an option that provides two different choices of interrupt triggering sensitivity. The $\overline{IRQ}$ pin contains an internal Schmitt trigger as part of its input to improve noise immunity. Refer to **Section 4. Interrupts** for more detail.